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APPLICATION FOR UNITED STATES PATENT

Title: METHOD FOR EVALUATING ANOMALIES IN A SEMICONDUCTOR MANUFACTURING PROCESS

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METHOD FOR EVALUATING ANOMALIES IN A SEMICONDUCTOR MANUFACTURING PROCESS

FIELD OF THE INVENTION

This invention relates, in general, to semiconductor manufacturing processes and, more particularly, to identifying process signatures of the semiconductor manufacturing process.

BACKGROUND OF THE INVENTION

It is well known that integrated circuits and discrete semiconductor devices are manufactured using a series of process steps. A typical semiconductor process flow may involve more than one hundred process steps including processes such as lithography, etching, doping, oxidation, planarization, metallization, passivation, and cleaning, among others. Although the process steps for manufacturing integrated circuits have been well characterized, a significant number of defects still appear on the semiconductor wafers. Events capable of causing these defects include, but are not limited to, particle contamination, scratching, polishing anomalies, wafer spinning processes, watermarks, particle stains, and micro-scratching. Making matters worse, semiconductor manufacturers are increasing the density of devices per die and increasing the size of the wafers to increase the number of die per wafer. Thus, a few defects on a wafer can significantly decrease the die yield on the wafer.

Hence, semiconductor manufacturers have incorporated inspection techniques using optical image devices capable of discerning unique defect patterns on a wafer surface, commonly referred to as defect spatial signatures. FIG. 1 is a wafer map 10 showing random defects on a semiconductor wafer. It should be noted that the distinguishing feature of a wafer map having random defects is the absence of any type of pattern or any defect spatial signatures. A problem with random defects is that finding the cause of the defects is extremely difficult. FIG. 2 is a wafer map 15 of a semiconductor wafer having a defect spatial signature caused by, for example, a wafer spinning process. Although the optical image devices allow engineers to view the defect spatial signatures on a wafer, it is

difficult for engineers to remember all the types of defect spatial signatures they have seen and associate a particular signature with a particular process step or piece of process equipment.

Accordingly, what is needed is a method to enable engineers to review a defect spatial signature and associate the signature with a specific process step or piece of process equipment.

SUMMARY OF THE INVENTION

The present invention satisfies the foregoing need by providing a method for performing defect spatial signature analysis. In a preferred embodiment, defect information and the associated identification information are stored in a relational database. A defect spatial signature for a newly inspected wafer is generated and the relational database is searched to determine if the new defect spatial signature matches any of the defect spatial signatures in the relational database. If a match occurs, the engineers are notified. The defect information and its associated wafer identification information are stored in the relational database.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which like references designate like elements and in which:

FIG. 1 is a wafer map lacking a defect spatial signature;

FIG. 2 is a wafer map illustrating a defect spatial signature;

FIG. 3 is a flow chart of a process for performing defect spatial signature analysis in accordance with an embodiment of the present invention; and

FIG. 4 is a wafer map illustrating a defect spatial signature having a clustering boundary.